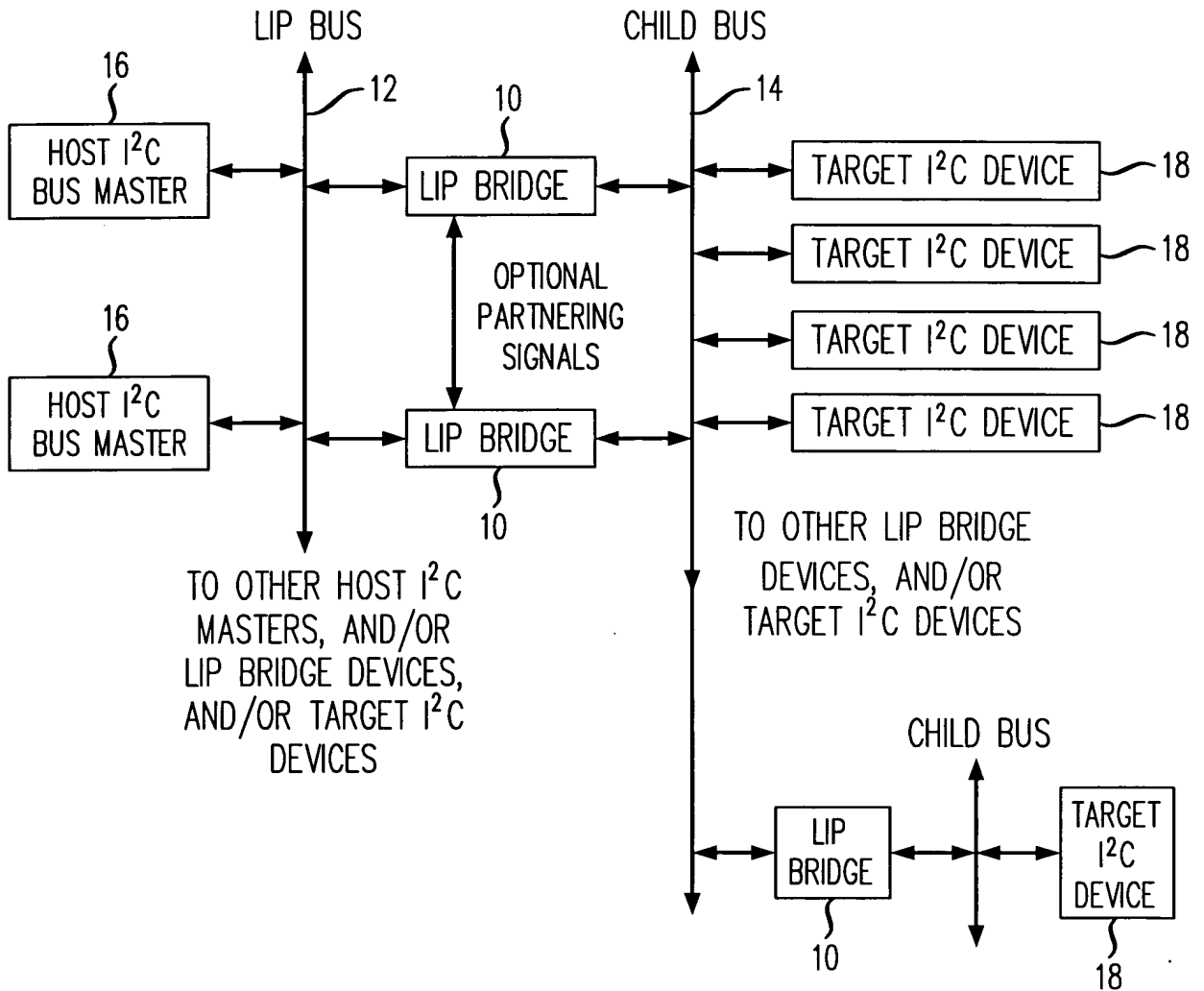




Drawing Approved
CCC 12/3/03

FIG. 1
TYPICAL LIP BRIDGE USAGE




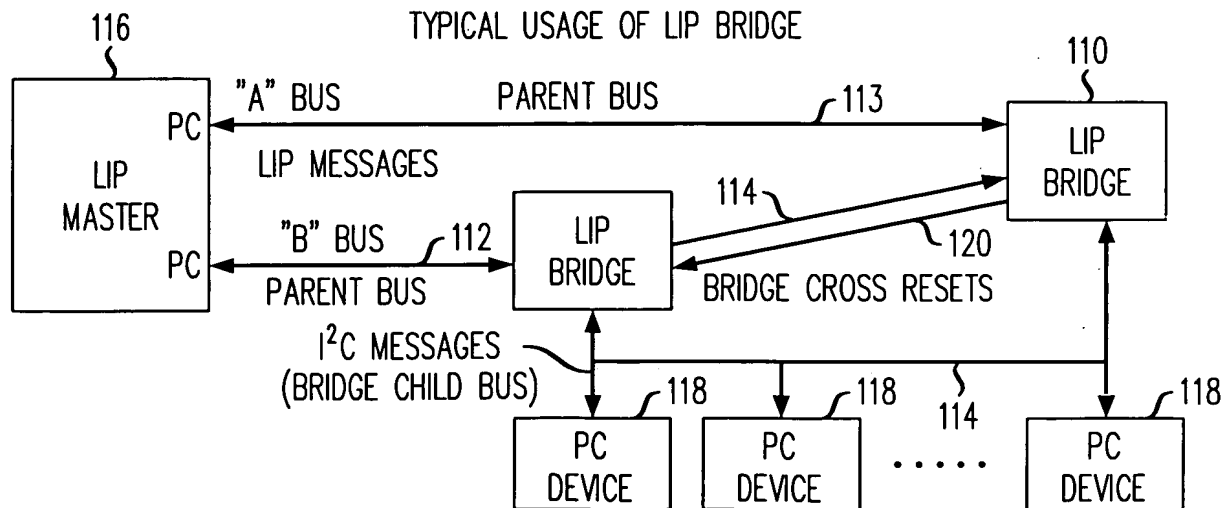


FIG. 2

The diagram illustrates the internal architecture of the LIP bridge, showing the flow of data and control signals between various components. Key elements include:

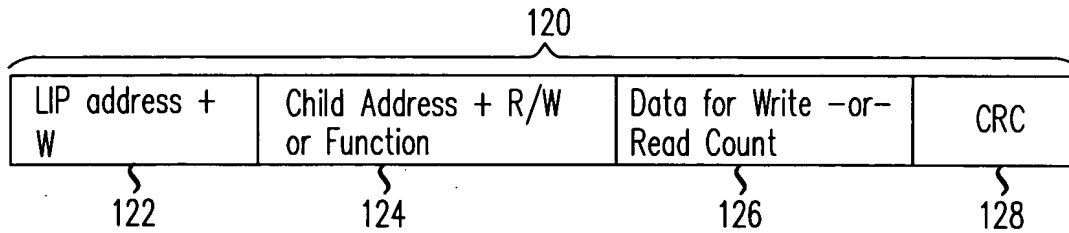
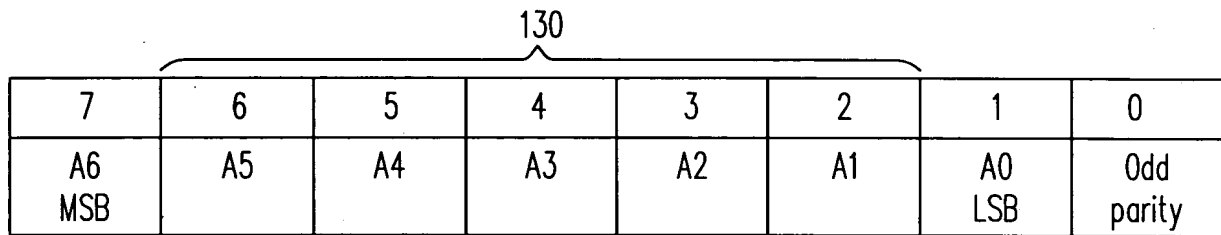
- Buses:** The LIP BUS (12) and CHILD BUS (14) are connected via the LIP BRIDGE (10).
- Transceivers:** The LIP BUS I²C TRANSCEIVER (20) and CHILD BUS I²C TRANSCEIVER (50) facilitate communication with external devices.
- Error Handling:** The ERROR LOG (41) and ERROR LOGGER (40) manage system errors. The COMMAND COLLISION DETECTION (38) block identifies conflicts in command execution.
- Control and Monitoring:** The GLOBAL RESET (42), GLOBAL WATCHDOG (44), LIP SUPPLY VOLTAGE MONITOR (46), and EVENT WATCHDOG TIMER (56) ensure system stability and proper operation.
- Data Flow:** Incoming LIP packets (30) are processed by the INCOMING LIP PACKET INCOMING FIFO (30) and the LIP PACKET PARSER&DISPATCH (32). Outgoing packets are managed by the OUTGOING LIP PACKET FIFO 0 (28) and OUTGOING LIP PACKET FIFO 1 (29).
- Special Function Command Engine (32):** This block handles special function commands and coordinates with the CHILD BUS COMMAND ENGINE (36) and the LIP PACKET PARSER&DISPATCH (32).

TYPICAL USAGE OF LIP BRIDGE



"Replacement Sheet"

3/13

**FIG. 4****FIG. 5**

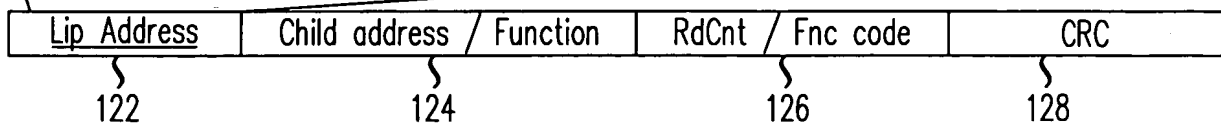
Hardware Address Strapping

FIG. 6

The LIP Address / Function encoding within the four byte LIP packet is as follows:

Lip address

7	6	5	4	3	2	1	0
A6 MSB	A5	A4	A3	A2	A1	A0 LSB	R/!W





4/13

FIG. 7

The Child Address / Function Encoding is as follows:

Child Address / Function

7	6	5	4	3	2	1	0
MSB	...					LSB	R/W

LIP Address	Child address / Function	Wr data / RdCnt / Fnc code	CRC
122	124	126	128

FIG. 8Read Count Field

7 MSB	6	5	4	3	2	1	0 LSB
Rsvd-0	SrclId	RdCnt					

LIP Address	Child Bus Address	Read Count field	CRC
122	124	126	128

FIG. 9Read Data Tag

7 MSB	6	5	4	3	2	1	0 LSB
No Data	SrclId	RdCnt					

138	136	134	
LIP Address + R	Read Data Tag	RdCnt data bytes	CRC
	132	130	142

FIG. 10Status Byte Register Organization

RAZ	RAZ	RAZ	ME	LBWE	LBRE	CBWE	CBRE
MSB							LSB

150



FIG. 11

TABLE 8

Key to Symbols	
Symbol	Meaning
S	I ² C bus start condition
P	I ² C bus stop condition
A	Acknowledge
A	No-Acknowledge
LA	LIP address
CA	Child bus address
W	R/W bit within address field is set for WRITE
R	R/W bit within address field is set for READ
CRC	CRC byte
Data	Data byte
Count	Read count
Fnc(x)	Special function command "x" - where x is the function's hex code
	Gray shade indicates data sent from Host Bus to LIP bridge
	White indicates data sent from LIP bridge to Master
.....	Zero or more instances of the preceding transaction.

Host bus master to LIP One Byte Child Bus Write

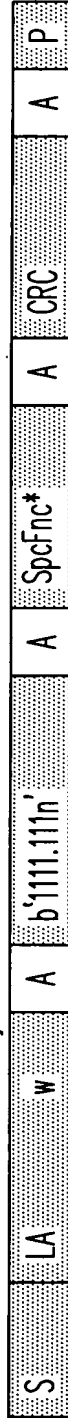


} 160



FIG. 12

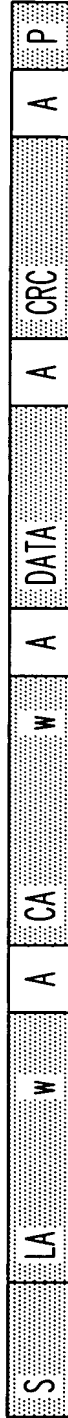
Host bus master to I²C Multi-Byte Write



* Child I²C start



.....



To complete transaction, either:



OR

Child I²C stop



Where: n=0 for host bus master 0 and n=1 for host bus master 1. The "***" CA field contains a different value than that contained in the first data packet (SECOND PACKET ABOVE). This can be either a different child address, or it can be a special function indicator of binary '1111.111n'.

162

FIG. 13

Special Function Action Returning Nor Requiring Data

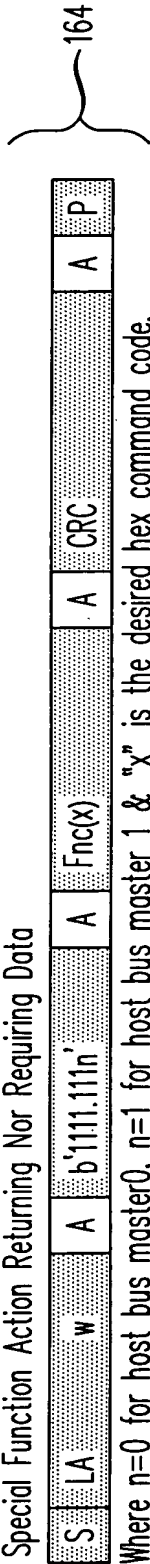


FIG. 14

Special Function Action Returning Data

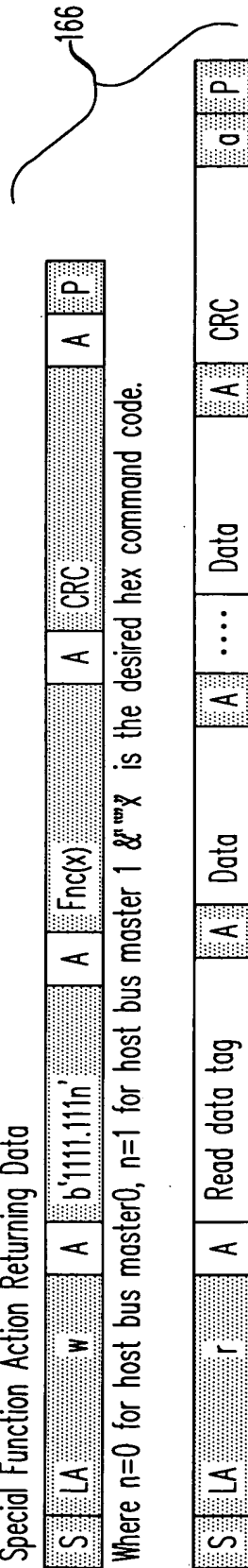


FIG. 15

Special Function Action Requiring Data

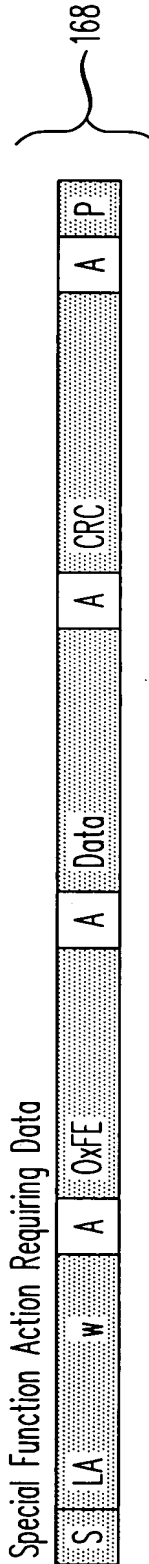
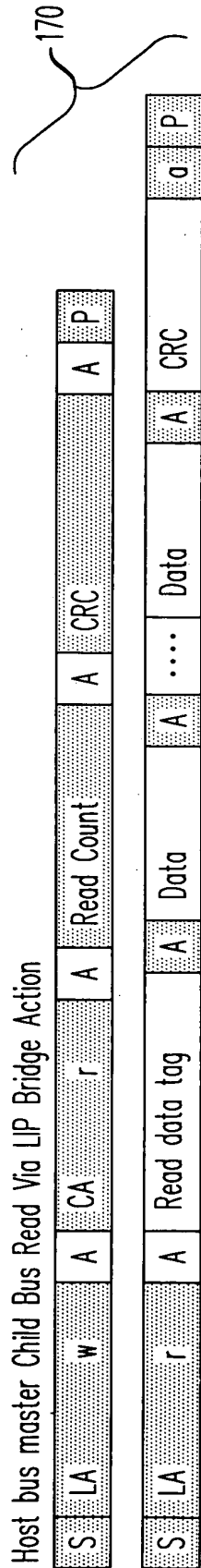


FIG. 16

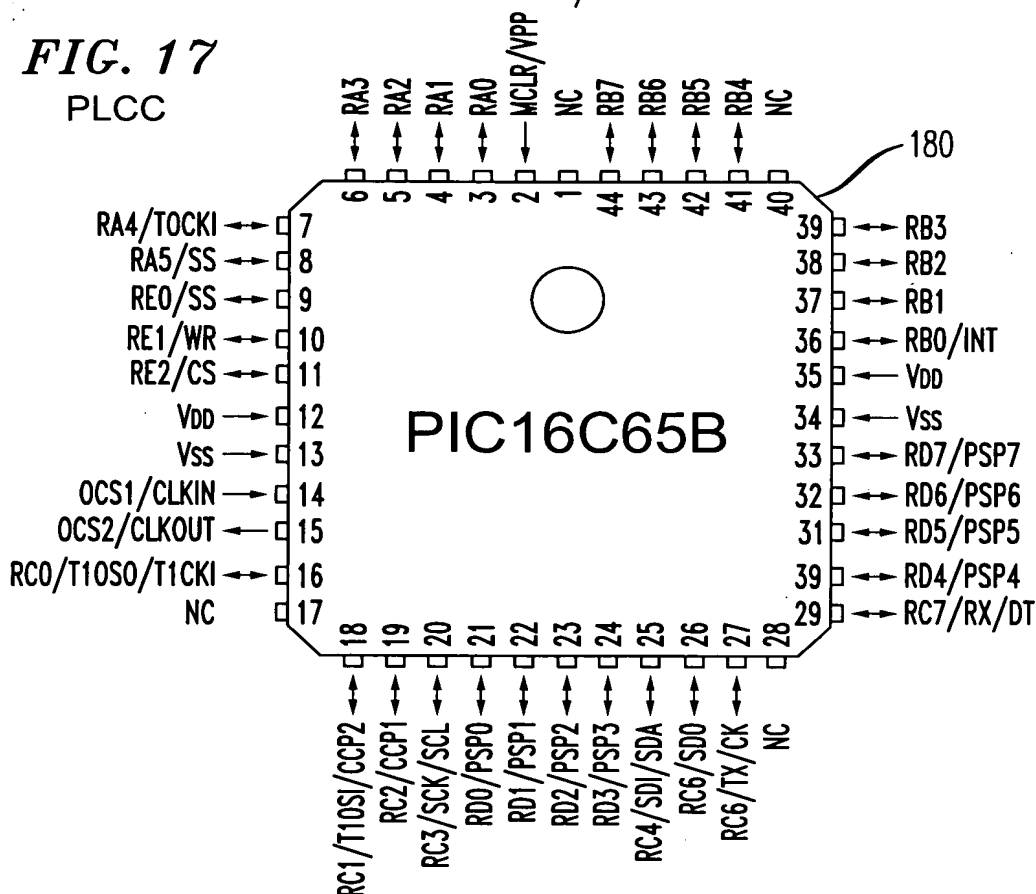
Host bus master Child Bus Read Via LIP Bridge Action



8/13

FIG. 17

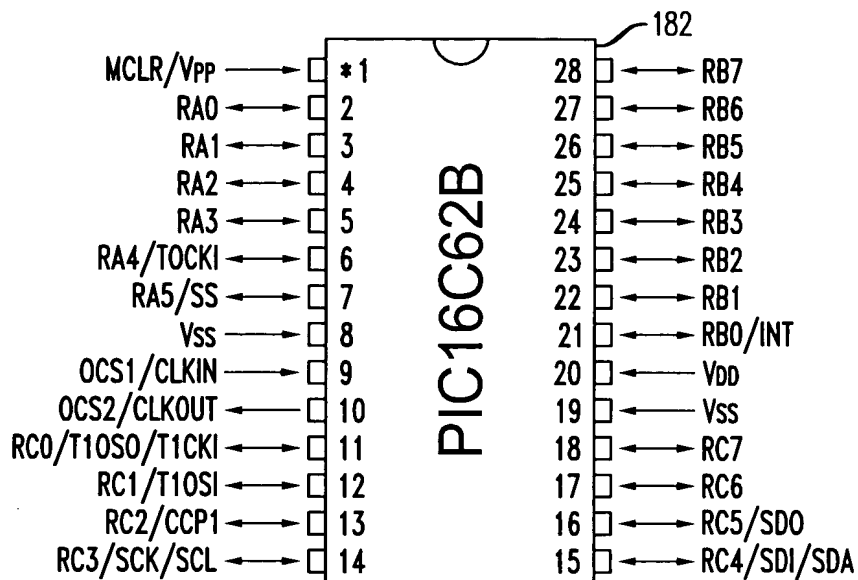
PLCC



PIN #	Label	Function
2	!MCLR	!partner_reset_in - Active low input for reset from partner LIP bridge (Also VPP pin for in circuit programming)
3	RA0	!partner_reset_out - Active low output to reset partner LIP bridge
20	RC3	LIP_clk - LIP bus serial clock in
25	RC4	LIP_data - LIP bus serial data in/out (bidirectional)
27	RC6	child_clk - child bus clock output
29	RC7	child_data - child bus data in/out (bidirectional)
37	RB1	LIP_addr_parity - parity bit for LIP address (strap to make odd parity)
38	RB2	LIP_addr0 - bit 0 to strap LIP I ² C address
39	RB3	LIP_addr1 - bit 1 to strap LIP I ² C address
41	RB4	LIP_addr2 - bit 2 to strap LIP I ² C address
42	RB5	LIP_addr3 - bit 3 to strap LIP I ² C address
4	RA1	LIP_addr4 - bit 4 to strap LIP I ² C address
5	RA2	LIP_addr5 - bit 5 to strap LIP I ² C address
43	RB6	In circuit programming clock
44	RB7	In circuit programming data
6	RA3	child_bus_busy_out - active low open collector output when this LIP bridge owns child bus (needs a 1K pull up to Vdd).
36	RB0	child_bus_busy_in - active low input when partner LIP bridge owns child bus



FIG. 18

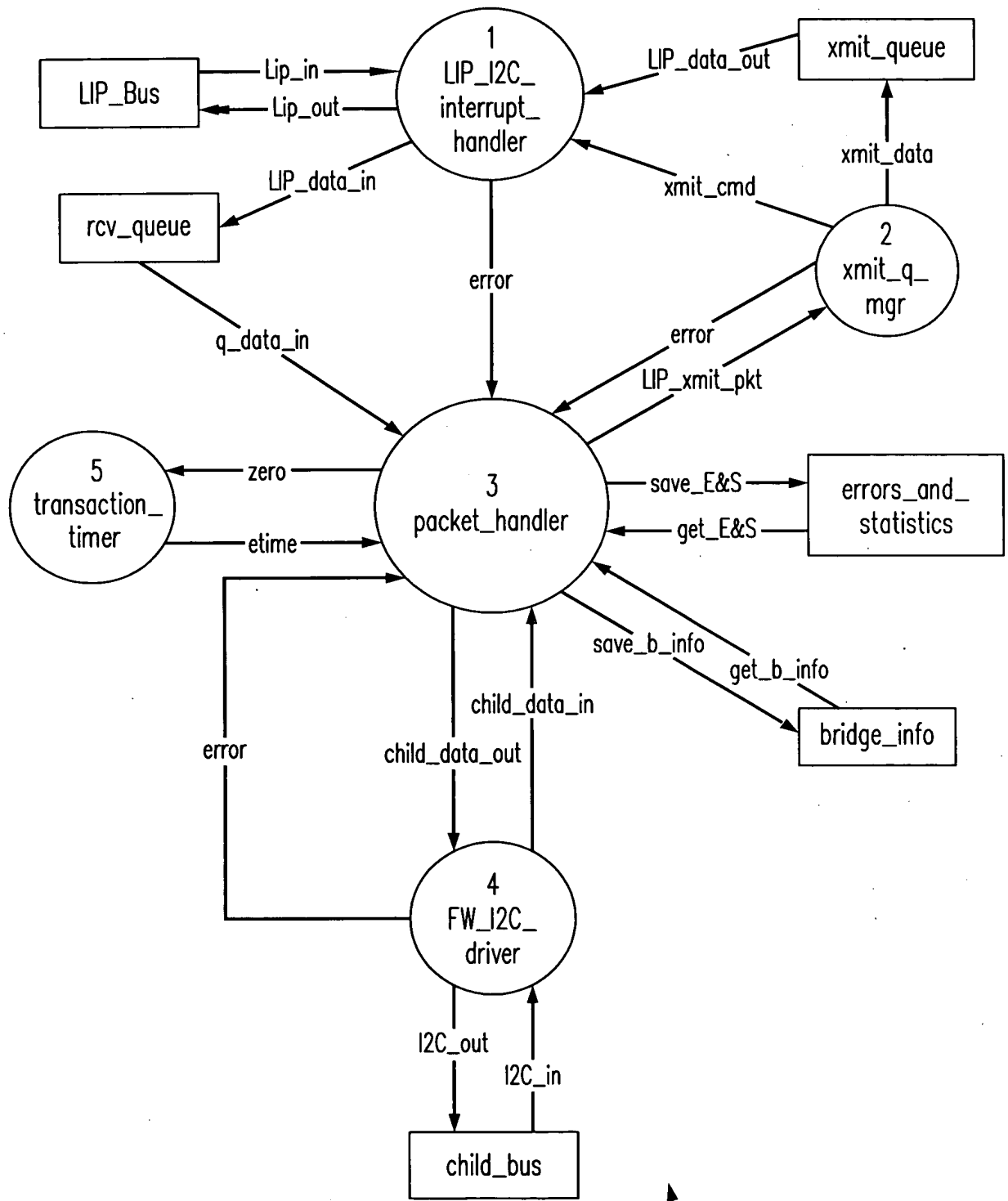


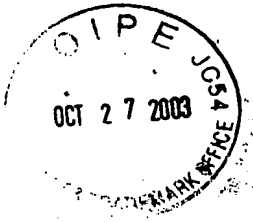
PIN #	Label	Function
1	!MCLR	!partner_reset_in - Active low input for reset from partner LIP bridge (Also VPP pin for in circuit programming)
2	RA0	!partner_reset_out - Active low output to reset partner LIP bridge
14	RC3	LIP_clk - LIP bus serial clock in
15	RC4	LIP_data - LIP bus serial data in/out (bidirectional)
17	RC6	child_clk - child bus clock output
18	RC7	child_data - child bus data in/out (bidirectional)
22	RB1	LIP_addr_parity - parity bit for LIP address (strap to make odd parity)
23	RB2	LIP_addr0 - bit 0 to strap LIP I ² C address
24	RB3	LIP_addr1 - bit 1 to strap LIP I ² C address
25	RB4	LIP_addr2 - bit 2 to strap LIP I ² C address
26	RB5	LIP_addr3 - bit 3 to strap LIP I ² C address
3	RA1	LIP_addr4 - bit 4 to strap LIP I ² C address
4	RA2	LIP_addr5 - bit 5 to strap LIP I ² C address
27	RB6	In circuit programming clock
28	RB7	In circuit programming data
5	RA3	child_bus_busy_out - active low output when this LIP bridge owns child bus (needs a 1K pull up to Vdd).
21	RB0	child_bus_busy_in - active low input when partner LIP bridge owns child bus



10/13

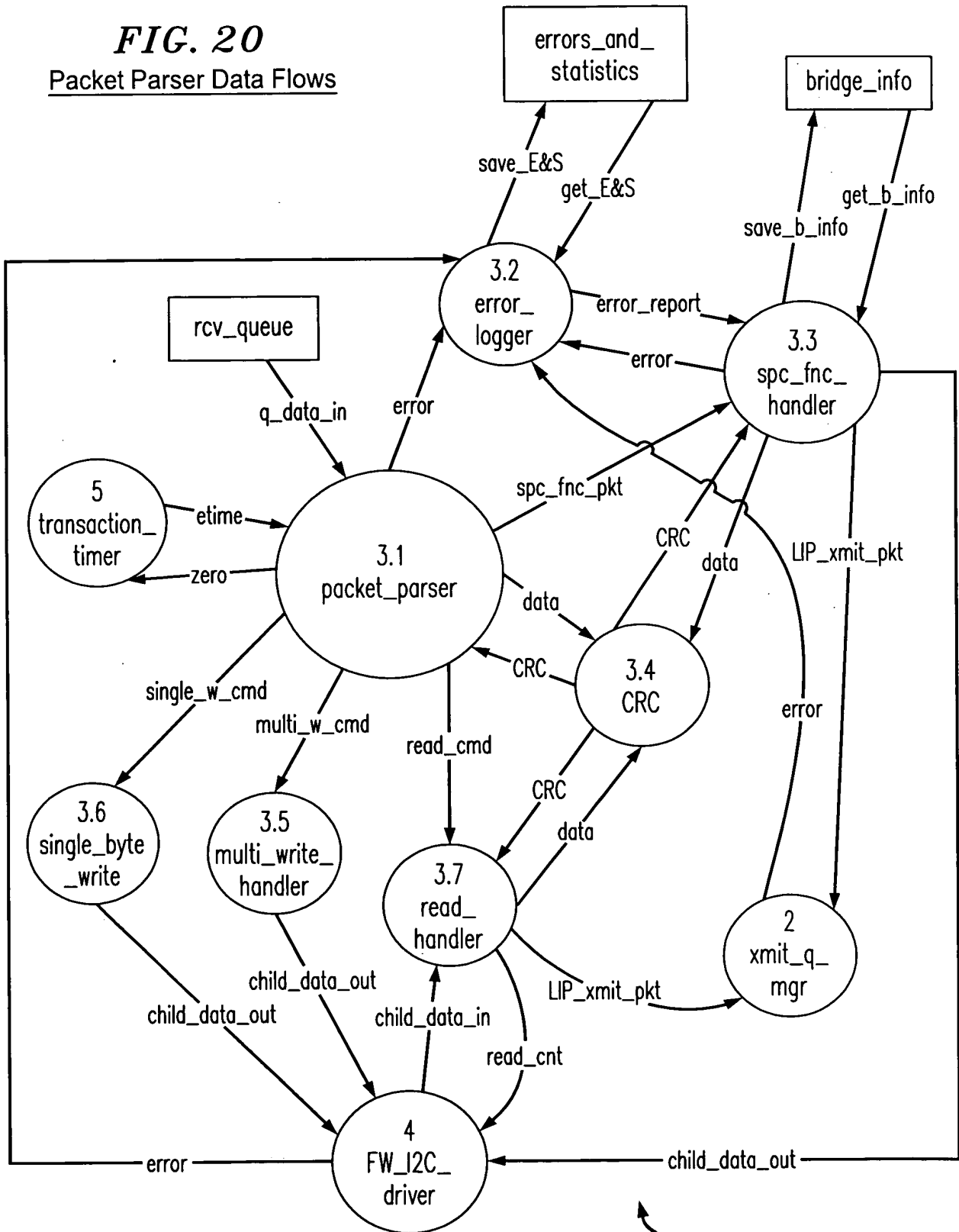
FIG. 19
Level 1 Data Flow Diagram





11/13

FIG. 20
Packet Parser Data Flows





12/13

FIG. 21

Firmware I2C Data Flows

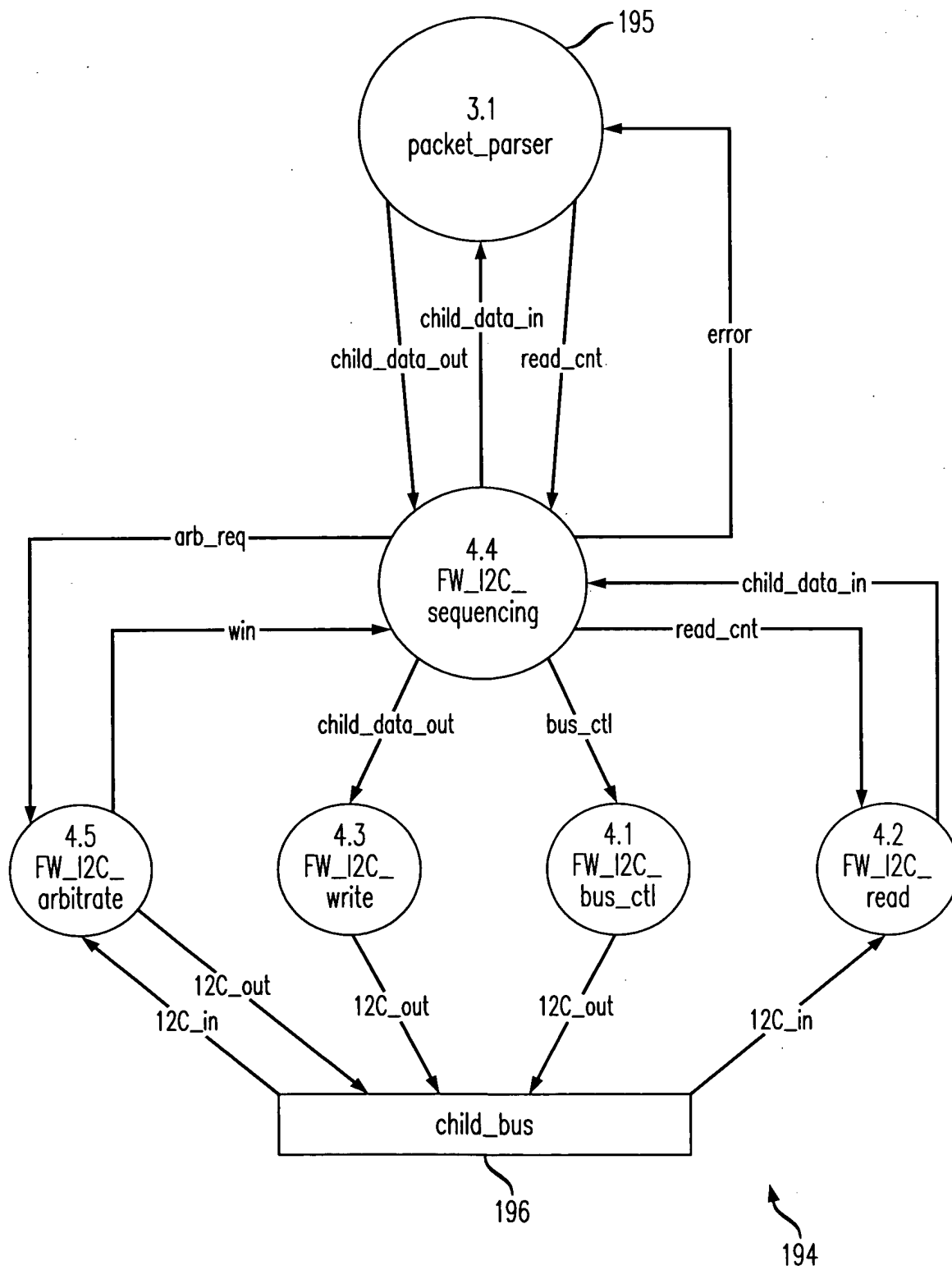




FIG. 22

